Notice of Allowability	Application No.	Applicant(s)	
	09/981,954	MEHTA ET AL.	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *September 11, 2006*.

2. ☒ The allowed claim(s) is/are *1-7,14-21 and 28-45*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Introduction

1. This communication is in response to the Applicant's communication dated September 11, 2006. Claims 1-7, 14-21 and 28-45 of the application are pending.

Examiner's Amendment

2. Authorization for this examiner's amendment was given in a telephone conversation by Mr. Shreen K. Danamraj on October 4, 2006.

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to the applicants, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

3. In the claims:

In claim 1, Lines 17-23, "wherein said second plurality of memory compilers are sampled from said first plurality of memory compilers such that each memory instance compiled by said second plurality of memory compilers corresponds to a respective congruent memory instance of said first parametric dataset having identical numbers of physical rows and physical columns"

has been changed to

-- wherein said second plurality of memory compilers are sparsely sampled from said first plurality of memory compilers such that each memory instance compiled by said second plurality of memory compilers corresponds to a respective congruent memory instance of said first parametric dataset having identical numbers of physical rows and physical columns, and said second plurality of memory compilers comprises a subset of said first plurality of memory compilers--.

In claim 16, Lines 18-23, "wherein said second plurality of memory compilers are sampled from said first plurality of memory compilers such that each memory instance compiled by said second plurality of memory compilers corresponds to a respective congruent memory instance of said first parametric dataset having identical numbers of physical rows and physical columns"

has been changed to

-- wherein said second plurality of memory compilers are sparsely sampled from said first plurality of memory compilers such that each memory instance compiled by said second plurality of memory compilers corresponds to a respective congruent memory instance of said first parametric dataset having identical numbers of physical rows and physical columns, and said second plurality of memory compilers comprises a subset of said first plurality of memory compilers--.

In claim 35, Line 12, "having identical numbers of physical rows and physical columns"

has been changed to

-- having identical numbers of physical rows and physical columns, and said second type of memory instances comprises a subset of said first type of memory instances --.

Reasons for Allowance

4. Claims 1-7, 14-21 and 28-45 of the application are allowed over prior art of record.

5. The following is an Examiner's statement of reasons for the indication of allowable subject matter:

The closest prior art of record shows:

(1) a memory compiler methodology including a stand alone memory interface (SAMI); the SAMI provides tools for interfacing with commercially available simulation software; the user selects the memory type such as SRAM, ROM, Dual port, synchronous or asynchronous memory; the SAMI tool generates possible memory configurations specifying rows, blocks, column multiplexing; then the characterization of the memory is done to derive the mathematical equations for key parameters and properties of the memory; a small number of configurations is selected to generate accurate sets of equations; for a three variable analysis, the corner points of a cube are selected defining the extreme combinations of the three variables e.g. bits per word, rows and column multiplexing factor; then a second set called Box-Benken scheme is selected consisting of central points of each edge of the cube; the center point of the cube is then added; all memory configurations with these combinations of parameters are simulated and the results

tabulated; multivariate regression models are fitted to show the dependent variables as functions of independent variables; the equations are developed for memory access time, cycle time, speed, power, size etc; these equations are used to determine the values of the dependent variables for other combinations of parameters used in the design of the memory; a table of all possible row, block and column multiplexing combinations that meet the user's requirements is then generated (**Djaja et al.**, U.S. Patent 6,405,160);

(2) an automatic memory characterization system for determining timing characteristics associated with a plurality of circuit instances of a memory design; the memory devices include SRAM, DRAM, ROM, EPROM and EEPROM; the memory compiler includes a characterization tool for determining the timing parameters for each memory instance; due to large number of memory instances possible, a small subset of possible combinations of design parameters is selected as white box timing model based on actual simulation results; a black box timing model for a particular instance of the memory design may be estimated using equations and look up tables based on timing models for other instances; the white box timing models are generated for corner instances of the memory design having the smallest and largest sizes of the memory array; black box timing models for memory instances having array sizes ranging between those characterized instances are determined by interpolation or using equations providing timing estimates (**Yuan et al.,** U.S. Patent 6,249,901); and

(3) a parameterized memory characterization system, PASTEL which extracts the characteristics of ASIC on-chip memories such as delay, timing and power consumption; it is a time consuming process to characterize parameterized memories in advance because they are larger in size and have many combinations of parameters; PASTEL is a fully automated process

from exact wire RC extraction through circuit reduction, input vector generation, waveform measurement, data sheet and library creation; PASTEL calculates the characteristics of memories under very tight error condition within a reasonable simulation time; the circuit reduction scheme cuts the non-active portion of the circuit with respect to the signal propagation of interest and merges loads to get simulation speeded up; PASTEL replaces the transistors and parasitic RCs by reduced order equivalent circuits; for power calculation the circuits are not reduced; the memory synthesizer generates the entire reduced order netlist of a memory of specified size (word, bit); an analytical method is used to get the timing constraints thus reducing the simulation time very much (**Ogawa et al.,** "PASTEL: A parametrized memory characterization system", IEEE, 1998).

Additional state of the art reviewed and considered by the Examiner is found in Gee et al., "A diffused CMOS SRAM compiler for gate arrays", IEEE 1991; and Zhang et al., "A multi-magabit memory compiler: Tomorrow's IP", IEEE 1999.

None of these references taken either alone or in combination with the prior art of record discloses a memory compiler characterization method for determining parametric data associated with compilable memory instances, specifically including:

(Claim 1) "obtaining a second parametric dataset by characterizing said particular parameter for a second set of memory instances that are compiled by a second plurality of memory compilers, each of said second plurality of memory compilers for compiling a respective memory instance organized with a second MUX factor, wherein said second plurality

of memory compilers are sparsely sampled from said first plurality of memory compilers such that each memory instance compiled by said second plurality of memory compilers corresponds to a respective congruent memory instance of said first parametric dataset having identical numbers of physical rows and physical columns, and said second plurality of memory compilers comprises a subset of said first plurality of memory compilers;

determining scale factors for a select number of parametric data points associated with respective congruent memory instances of said first and second parametric datasets;

obtaining an interpolated scale factor based on said scale factors; and

deriving a value of said particular parameter for an additional memory instance having said second MUX factor by applying said interpolated scale factor to a data point associated with a memory instance having said first MUX factor, wherein said memory instance with said first MUX factor is congruent with respect to said additional memory instance with said second MUX factor".

None of these references taken either alone or in combination with the prior art of record discloses a memory compiler characterization method for determining parametric data associated with compilable memory instances, specifically including:

(Claim 16) "obtaining a second parametric dataset by characterizing said particular parameter for a second set of memory instances compiled by a second plurality of memory compilers that are representative of a second memory technology, each of said second plurality of memory compilers for compiling a respective memory instance organized with said select MUX factor, wherein said second plurality of memory compilers are sparsely sampled from said

first plurality of memory compilers such that each memory instance compiled by said second plurality of memory compilers corresponds to a respective congruent memory instance of said first parametric dataset having identical numbers of physical rows and physical columns, and said second plurality of memory compilers comprises a subset of said first plurality of memory compilers;

determining scale factors for a select number of parametric data points associated with respective congruent memory instances of said first and second parametric datasets;

obtaining an interpolated scale factor based on said scale factors; and

deriving a value of said particular parameter for an additional memory instance of said second memory technology by applying said interpolated scale factor to a data point associated with a memory instance of said first memory technology, wherein said memory instance of said first memory technology is congruent with respect to said additional memory instance of said second memory technology".

None of these references taken either alone or in combination with the prior art of record discloses a memory compiler characterization system, specifically including:

(Claim 35) "means for characterizing a second plurality of memory compilers with respect to said particular parameter, said second plurality of memory compilers for compiling memory instances of a second type, wherein said memory instances of second type comprise memory instances sparsely sampled from said memory instances of first type such that each sampled memory instance of second type corresponds to a respective congruent memory instance

of first type having identical numbers of physical rows and physical columns, and said second type of memory instances comprises a subset of said first type of memory instances;

means for determining scale factors between values of said particular parameter respectively associated with a pair of congruent memory instances of said first and second types;

an interpolator to obtain an interpolated scale factor based on said scale factors; and

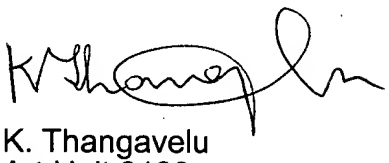
means for obtaining a value of said particular parameter for an additional memory instance of second type by utilizing said interpolated scale factor in conjunction with a parametric value of a congruent memory instance of first type which corresponds to said additional memory instance".

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez, can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.



K. Thangavelu
Art Unit 2123
October 4, 2006